SEMICONDUCTOR MEMORY DEVICES AND MEMORY SYSTEMS INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This US non-provisional application claims the benefit of priority under 35 USC §119 to Korean Patent Application No. 10-2015-0106945, filed on Jul. 29, 2015, in the Korean Intellectual Property Office, the content of which is incorporated by reference herein in its entirety.

BACKGROUND

[0002] The present disclosure relates to semiconductor memory devices and memory systems including the same.

[0003] Semiconductor memory devices may be classified into non-volatile memory devices such as flash memory devices and volatile memory devices such as dynamic random access memories (DRAMs). The volatile memory devices such as DRAMs are commonly employed as system memories for mass data, because DRAMs are inexpensive. Manufacturing processes are scaled in the volatile memory devices such as DRAMs for increasing memory density. In addition, in DRAMs, a unit of a write/read operation is different from a unit of error correction code (ECC) encoding/ECC decoding using the ECC.

SUMMARY

[0004] It is an aspect to provide a semiconductor memory device, capable of reducing overhead.

[0005] It is another aspect to provide a memory system including the semiconductor memory device, capable of reducing overhead.

[0006] According to an aspect of an exemplary embodiment, there is provided a semiconductor memory device comprising a memory cell array including a plurality of memory cells; an input/output (I/O) gating circuit configured to, before performing a normal memory operation on the memory cell array by a first unit, perform a cell data initializing operation by writing initializing bits in the memory cell array by a second unit different from the first unit; and an error correction circuit configured to perform an error correction code (ECC) encoding and an ECC decoding on a target page of the memory cell array by the second unit, based on the initializing bits.

[0007] The first unit may correspond to a prefetching unit of the semiconductor memory device when the semiconductor memory device performs a read operation or a write operation, the second unit may correspond to a codeword unit of the semiconductor memory device, and the codeword unit is greater than the prefetching unit.

[0008] The I/O gating circuit may perform the cell data initializing operation in response to an initializing write command from an external device.

[0009] The I/O gating circuit may perform the cell data initializing operation in response to a power-up signal from an external device.

[0010] The semiconductor memory device may further comprise a register that stores a plurality of subsets and provides one of the subsets as the initializing bits in response to an initializing start signal; and a control logic circuit configured to output the initializing start signal to the register in response to one of an initializing write command from an external device and a power-up signal from the external device.

[0011] The initializing bits may have one of a first logic level and a second logic level different from the first logic level.

[0012] The control logic circuit may be configured to generate a first control signal to control the I/O gating circuit and a second control signal to control the error correction circuit in response to one of the initializing write command and the power-up signal.

[0013] When the semiconductor memory device performs a write operation to write a write data by the second unit from an external device in the target page after performing the cell data initializing operation, the error correction circuit may read a reset codeword by the second unit from the target page, the reset codeword including a reset main data and a reset parity data, the reset main data and the reset parity data including the initializing bits; correct at least one error in the reset main data using the reset parity data; and generate a write parity data based on the write data and a portion of the reset main data, and the I/O gating circuit may write the write data and the write parity data in the target page.

[0014] The error correction circuit may comprise an ECC encoder configured to read the reset codeword to correct the at least one error in the reset main data; and an ECC decoder configured to generate the write parity data based on the write data and some of the reset main data.

[0015] The target page may include a normal region that stores the main data and a parity region that stores the write parity data.

[0016] Each of the memory cells may include one of a dynamic memory cell and a resistive type memory cell.

[0017] The I/O gating circuit may be configured to perform the cell data initializing operation during a power-up sequence of the semiconductor memory device.

[0018] According to another aspect of an exemplary embodiment, there is provided a memory system comprising at least one semiconductor memory device; and a memory controller configured to control the at least one semiconductor memory device, wherein the at least one semiconductor memory device comprises a memory cell array including a plurality of memory cells; an input/output (I/O) gating circuit configured to, before performing a normal memory operation on the memory cell array by a first unit, perform a cell data initializing operation by writing initializing bits in the memory cell array by a second unit different from the first unit; and an error correction circuit configured to perform an error correction code (ECC) encoding and an ECC decoding on a target page of the memory cell array by the second unit, based on the initializing bits.

[0019] The first unit may correspond to a prefetching unit of the semiconductor memory device when the semiconductor memory device performs a read operation or a write operation, the second unit may correspond to a codeword unit of the semiconductor memory device, the codeword unit is greater than the prefetching unit, and the memory cell array is a three-dimensional memory cell array.

[0020] The at least one semiconductor memory device may include a plurality of semiconductor memory devices mounted on a module board, the memory controller may apply one of an initializing write command and a power-up signal to each of the semiconductor memory devices, and